1.7-W MONO FULLY DIFFERENTIAL AUDIO POWER AMPLIFIER

FEATURES

- Designed for Wireless or Cellular Handsets and PDAs
- 1.7 W Into 8 Ω From a 5-V Supply at THD = 10% (Typ)
- Low Supply Current: 4 mA typ at 5 V
- Shutdown Current: 0.01 μA Typ
- Fast Startup With Minimal Pop
- Only Three External Components
  - Improved PSRR (–80 dB) and Wide Supply Voltage (2.5 V to 5.5 V) for Direct Battery Operation
  - Fully Differential Design Reduces RF Rectification
  - –63 dB CMRR Eliminates Two Input Coupling Capacitors
- Pin to Pin Compatible With TPA2005D1 and TPA6211A1 in QFN Package
- Available in 3 mm X 3 mm QFN Package (DRB)

APPLICATIONS

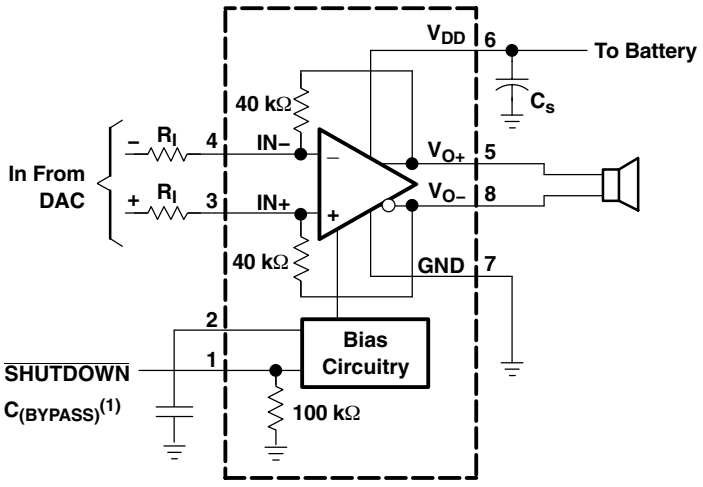
- Ideal for Wireless Handsets
- PDAs
- Notebook Computers

DESCRIPTION

The TPA6204A1 is a 1.7-W mono fully-differential amplifier designed to drive a speaker with at least 8-Ω impedance while consuming only 20 mm^2 total printed-circuit board (PCB) area in most applications. The device operates from 2.5 V to 5.5 V, drawing only 4 mA of quiescent supply current. The TPA6204A1 is available in the space-saving 3 mm x 3 mm QFN (DRB) package.

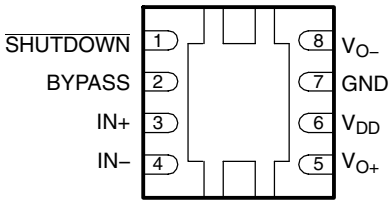
The TPA6204A1 is ideal for PDA/smart phone applications due to features such as –80-dB supply voltage rejection from 20 Hz to 2 kHz, improved RF rectification immunity, small PCB area, and a fast startup with minimal pop.

APPLICATION CIRCUIT

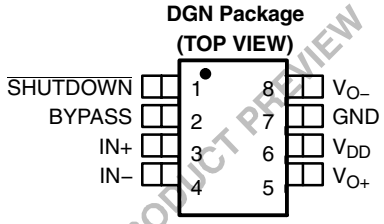


(1) $C_{(BYPASS)}$ is optional.

8-pin QFN (DRB) PACKAGE
(TOP VIEW)



DGN Package
(TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

	PACKAGED DEVICE	
	QFN (DRB)	MSOP (DGN)
Device	TPA6204A1DRB	TPA6204A1DGN
Symbolization	AYJ	TBD

(1) The DRB is only available taped and reeled. To order taped and reeled parts, add the suffix R to the part number (TPA6204A1DRBR).

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	DRB		
IN–	4	I	Negative differential input
IN+	3	I	Positive differential input
V_{DD}	6	I	Power supply
V_{O+}	5	O	Positive BTL output
GND	7	I	High-current ground
$V_{O–}$	8	O	Negative BTL output
$\overline{\text{SHUTDOWN}}$	1	I	Shutdown terminal (active low logic)
BYPASS	2		Mid-supply voltage, adding a bypass capacitor improves PSRR
Thermal Pad	–	–	Connect to ground. Thermal pad must be soldered down in all applications to properly secure device on the PCB.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Supply voltage, V_{DD}		–0.3 V to 6 V
Input voltage, V_I		–0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation		See Dissipation Rating Table
Operating free-air temperature, T_A		–40°C to 85°C
Junction temperature, T_J		–40°C to 150°C
Storage temperature, T_{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds	DRB	260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1)	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DRB	2.7 W	21.8 mW/°C	1.7 W	1.4 W

(1)) Derating factor based on high-k board layout.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}		2.5		5.5	V
High-level input voltage, V_{IH}	$\overline{\text{SHUTDOWN}}$	1.55			V
Low-level input voltage, V_{IL}	$\overline{\text{SHUTDOWN}}$			0.5	V
Operating free-air temperature, T_A		–40		85	°C

ELECTRICAL CHARACTERISTICS, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Output offset voltage (measured differentially)	V_I = 0 V differential, Gain = 1 V/V, V_{DD} = 5.5 V		–9	0.3	9	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V			–85	–60	dB
V_{IC}	Common mode input range	V_{DD} = 2.5 V to 5.5 V		0.5		V_{DD}–0.8	V
CMRR	Common mode rejection ratio	V_{DD} = 5.5 V, V_{IC} = 0.5 V to 4.7 V			–63	–40	dB
		V_{DD} = 2.5 V, V_{IC} = 0.5 V to 1.7 V			–63	–40	
	Low-output swing	R_L = 8 Ω, Gain = 1 V/V, V_{IN+} = V_{DD}, $V_{IN–}$ = 0 V or V_{IN+} = 0 V, $V_{IN–}$ = V_{DD}	V_{DD} = 5.5 V		0.45		V
			V_{DD} = 3.6 V		0.37		
			V_{DD} = 2.5 V		0.26	0.4	
	High-output swing	R_L = 8 Ω, Gain = 1 V/V, V_{IN+} = V_{DD}, $V_{IN–}$ = 0 V or $V_{IN–}$ = V_{DD}, V_{IN+} = 0 V	V_{DD} = 5.5 V		4.95		V
			V_{DD} = 3.6 V		3.18		
			V_{DD} = 2.5 V	2	2.13		
$\lvert I_{IH} \rvert$	High-level input current, $\overline{\text{SHUTDOWN}}$	V_{DD} = 5.5 V, V_I = 5.8 V			58	100	μA
$\lvert I_{IL} \rvert$	Low-level input current, $\overline{\text{SHUTDOWN}}$	V_{DD} = 5.5 V, V_I = –0.3 V			3	100	μA
I_Q	Quiescent current	V_{DD} = 2.5 V to 5.5 V, no load			4	6	mA
$I_{(SD)}$	Supply current	$V(\overline{\text{SHUTDOWN}})$ ≤ 0.5 V, V_{DD} = 2.5 V to 5.5 V, R_L = 8 Ω			0.01	1	μA
	Gain	R_L = 8 Ω		$\frac{38\ k\Omega}{R_I}$	$\frac{40\ k\Omega}{R_I}$	$\frac{42\ k\Omega}{R_I}$	V/V
	Resistance from shutdown to GND				100		kΩ

OPERATING CHARACTERISTICS, T_A = 25°C, Gain = 1 V/V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD + N= 1%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.36		W
			V_{DD} = 3.6 V		0.72		
			V_{DD} = 2.5 V		0.33		
		THD + N= 10%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.7		W
			V_{DD} = 3.6 V		0.85		
			V_{DD} = 2.5 V		0.4		
THD+N	Total harmonic distortion plus noise	V_{DD} = 5 V, P_O = 1 W, R_L = 8 Ω, f = 1 kHz			0.02%		
		V_{DD} = 3.6 V, P_O = 0.5 W, R_L = 8 Ω, f = 1 kHz			0.02%		
		V_{DD} = 2.5 V, P_O = 200 mW, R_L = 8 Ω, f = 1 kHz			0.03%		
k_{SVR}	Supply ripple rejection ratio	V_{DD} = 3.6 V, Inputs ac-grounded with C_i = 2 μF, $V_{(RIPPLE)}$ = 200 mV_{pp}	f = 217 Hz		–80		dB
			f = 20 Hz to 20 kHz		–70		
SNR	Signal-to-noise ratio	V_{DD} = 5 V, P_O = 1 W, R_L = 8 Ω			105		dB
V_n	Output voltage noise	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, Inputs ac-grounded with C_i = 2 μF	No weighting		15		μV_{RMS}
			A weighting		12		
CMRR	Common mode rejection ratio	V_{DD} = 3.6 V, V_{IC} = 1 V_{pp}	f = 217 Hz		–65		dB
R_F	Feedback resistance			38	40	44	kΩ
	Start-up time from shutdown	V_{DD} = 3.6 V, C_{BYPASS} = 0.1 μF			27		ms

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
P_O	Output power	vs Supply voltage	1
		vs Load resistance	2
P_D	Power dissipation	vs Output power	3
THD+N	Total harmonic distortion + noise	vs Output power	4
		vs Frequency	5
		vs Common-mode input voltage	6
K_{SVR}	Supply voltage rejection ratio	vs Frequency	7
	GSM Power supply rejection	vs Time	8
	GSM Power supply rejection	vs Frequency	9
	Closed loop gain/phase	vs Frequency	10
	Open loop gain/phase	vs Frequency	11
I_{DD}	Supply current	vs Supply voltage	12
		vs Shutdown voltage	13
	Start-up time	vs Bypass capacitor	14

OUTPUT POWER vs SUPPLY VOLTAGE

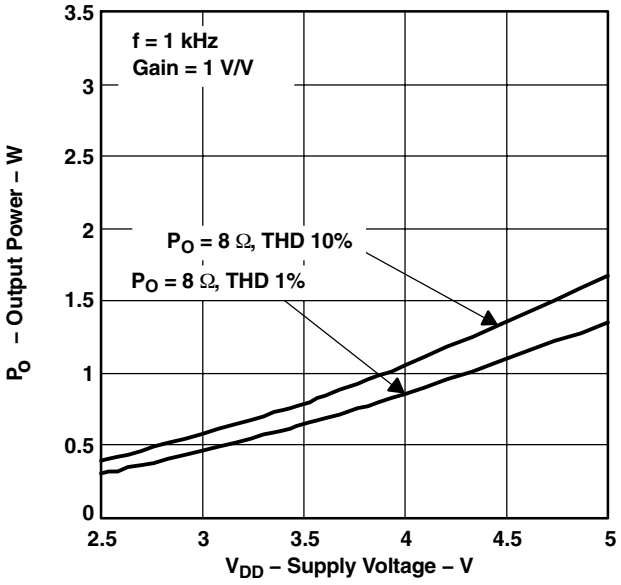


Figure 1

OUTPUT POWER vs LOAD RESISTANCE

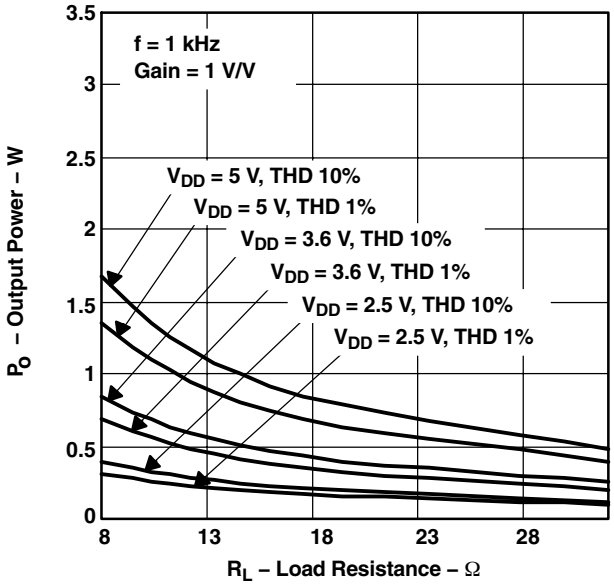


Figure 2

POWER DISSIPATION vs OUTPUT POWER

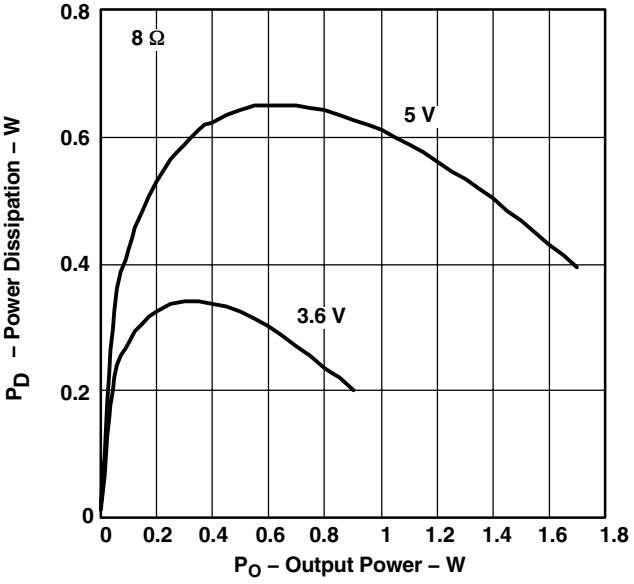


Figure 3

TOTAL HARMONIC DISTORTION + NOISE vs COMMON MODE INPUT VOLTAGE

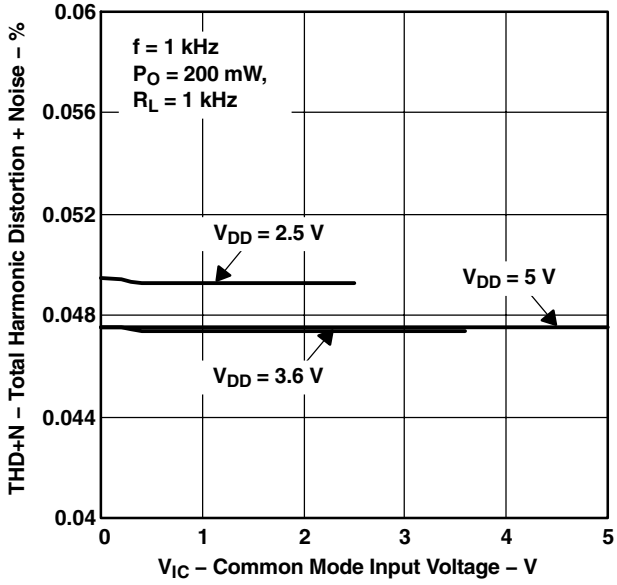


Figure 4

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

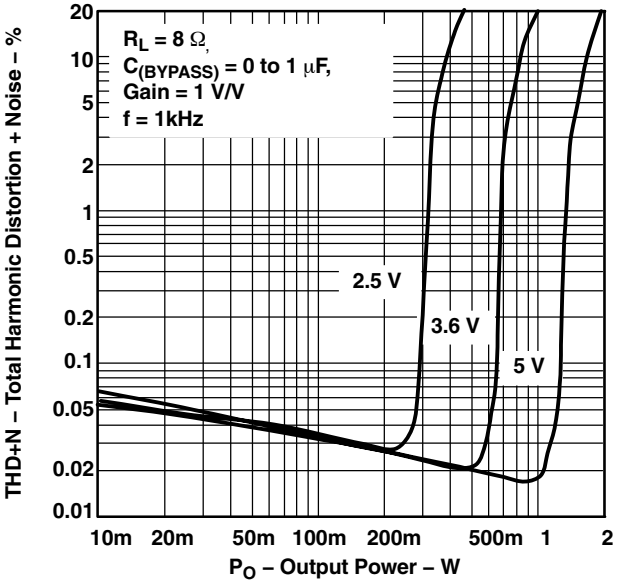


Figure 5

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

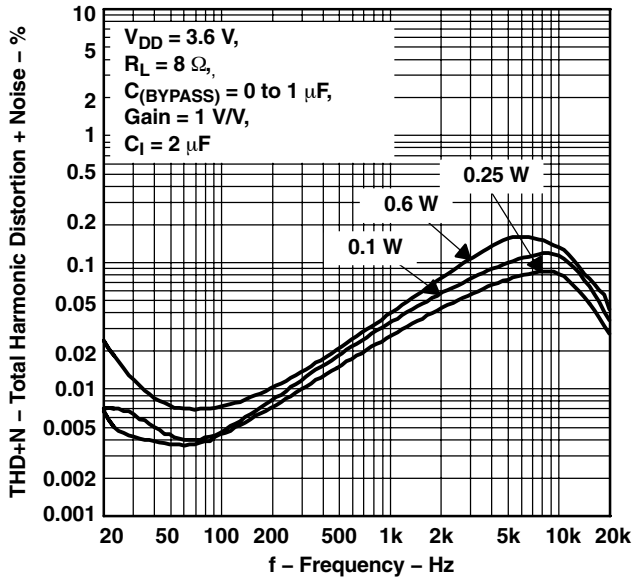


Figure 6

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

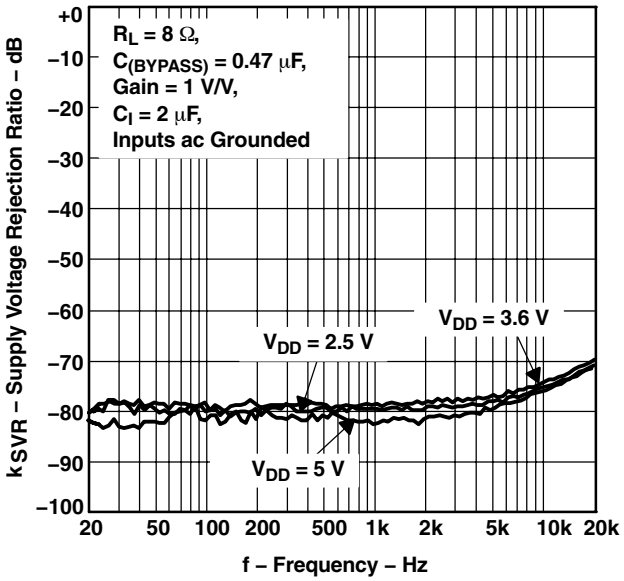


Figure 7

GSM POWER SUPPLY REJECTION vs FREQUENCY

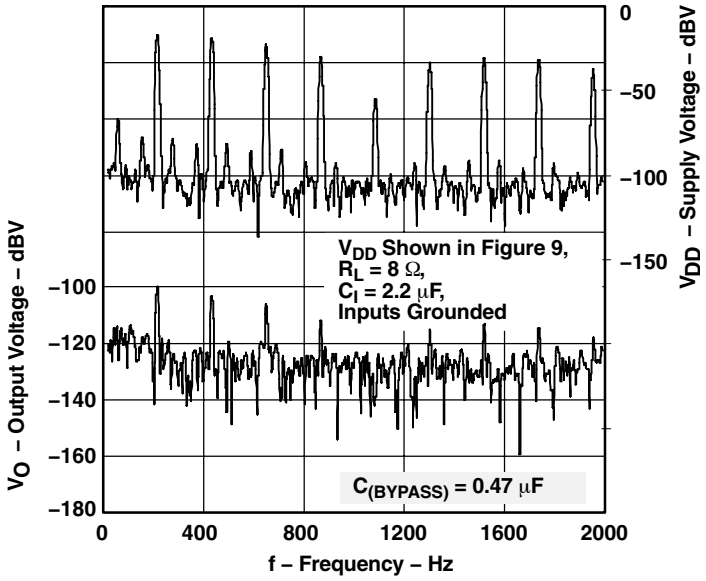


Figure 8

GSM POWER SUPPLY REJECTION vs TIME

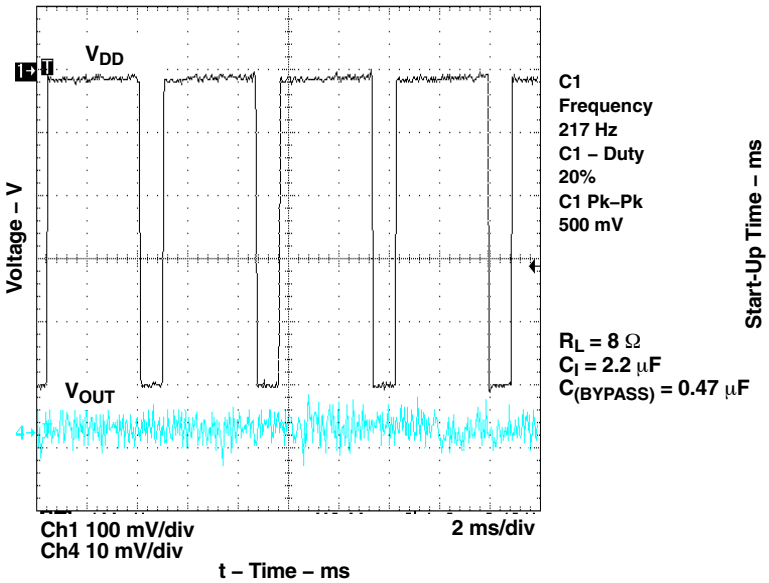


Figure 9

START-UP TIME vs BYPASS CAPACITOR

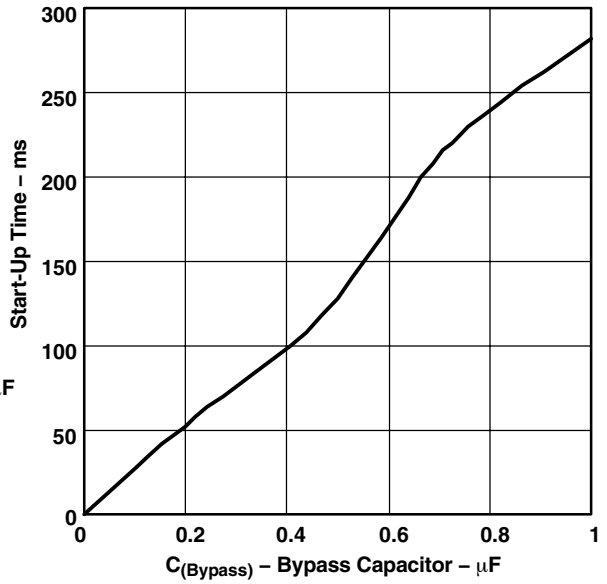


Figure 10

CLOSED LOOP GAIN/PHASE vs FREQUENCY

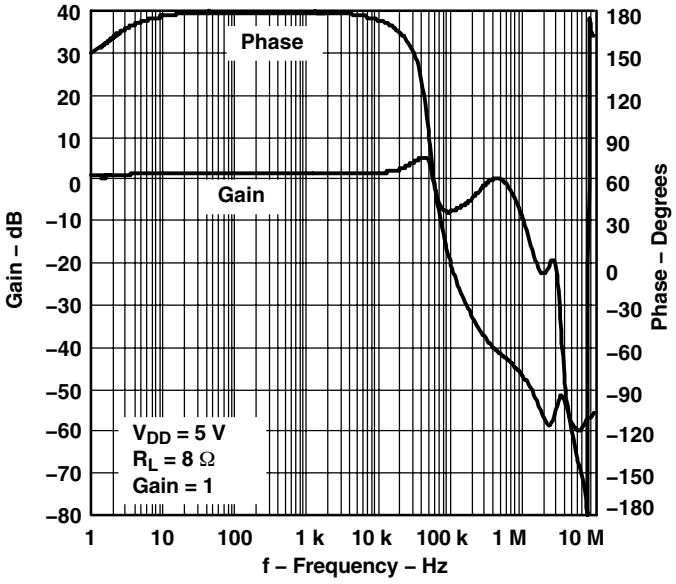


Figure 11

OPEN LOOP GAIN/PHASE vs FREQUENCY

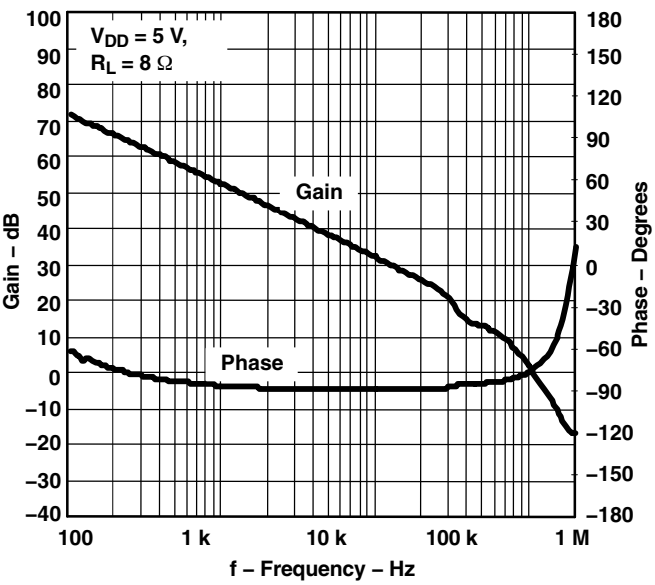


Figure 12

SUPPLY CURRENT vs SUPPLY VOLTAGE

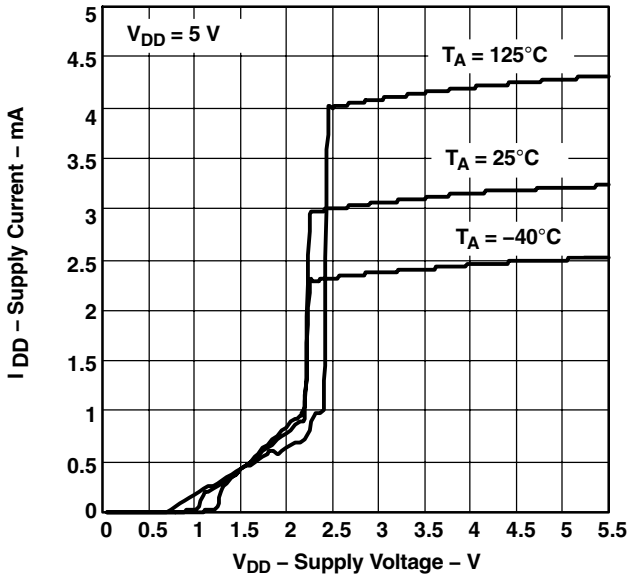


Figure 13

SUPPLY CURRENT vs SHUTDOWN VOLTAGE

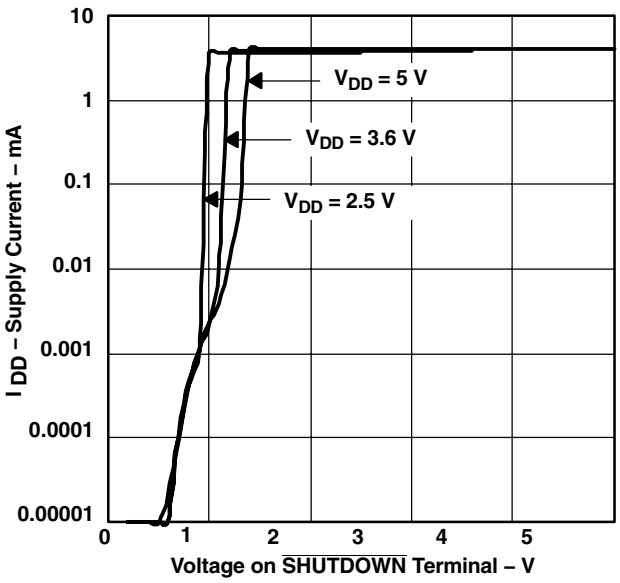


Figure 14

APPLICATION INFORMATION

FULLY DIFFERENTIAL AMPLIFIER

The TPA6204A1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input.

Advantages of Fully Differential Amplifiers

- **Input coupling capacitors not required:** A fully differential amplifier with good CMRR, like the TPA6204A1, allows the inputs to be biased at voltage other than mid-supply. For example, if a DAC has mid-supply lower than the mid-supply of the TPA6204A1, the common-mode feedback circuit adjusts for that, and the TPA6204A1 outputs are still biased at mid-supply of the TPA6204A1. The inputs of the TPA6204A1 can be biased from 0.5 V to V_{DD} – 0.8 V. If the inputs are biased outside of that range, input coupling capacitors are required.
- **Mid-supply bypass capacitor, $C_{(BYPASS)}$, not required:** The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid- supply affects both positive and negative channels equally and cancels at the differential output. However, removing the bypass capacitor slightly worsens power supply rejection ratio (k_{SVR}), but a slight decrease of k_{SVR} may be acceptable when an additional component can be eliminated.
- **Better RF-immunity:** GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

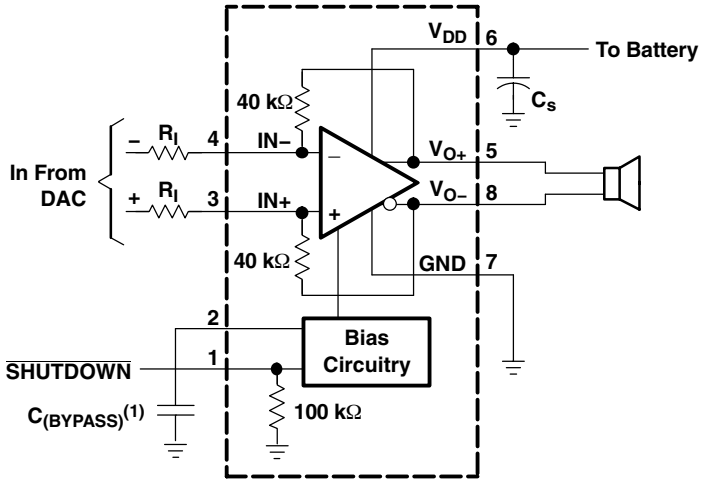
APPLICATION SCHEMATICS

Figure 15 through Figure 17 show application schematics for differential and single-ended inputs. Typical values are shown in Table 1.

Table 1. Typical Component Values

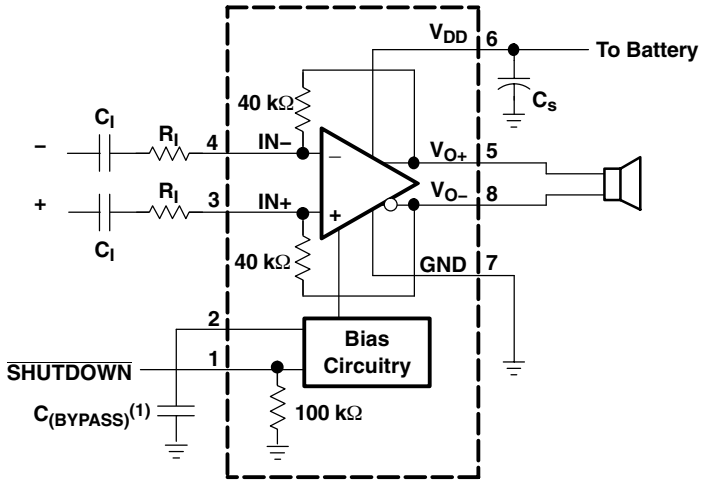
COMPONENT	VALUE
R_I	40 kΩ
$C_{(BYPASS)}$(1)	0.22 μF
C_S	1 μF
C_I	0.22 μF

(1) $C_{(BYPASS)}$ is optional



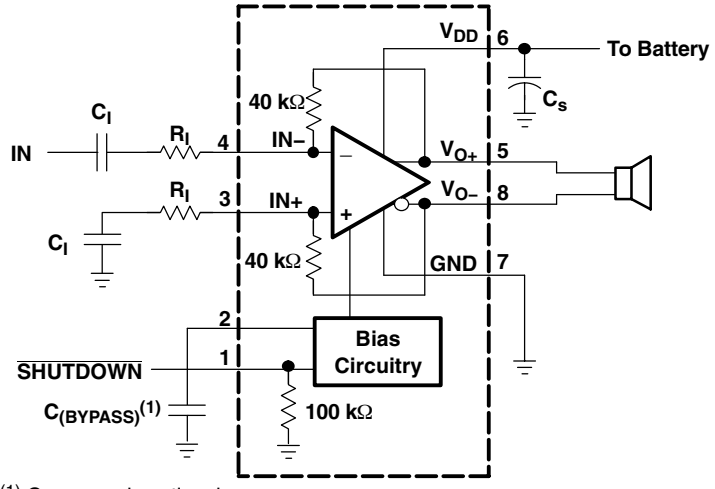
(1) $C_{(BYPASS)}$ is optional

Figure 15. Typical Differential Input Application Schematic



(1) $C_{(BYPASS)}$ is optional

Figure 16. Differential Input Application Schematic Optimized With Input Capacitors



(1) $C_{(BYPASS)}$ is optional

(2) Due to the fully differential design of this amplifier, the performance is severly degraded if you connect the unused input to **BYPASS** when using single-ended inputs.

Figure 17. Single-Ended Input Application Schematic

SELECTING COMPONENTS

Resistors (R_I)

The input resistor (R_I) can be selected to set the gain of the amplifier according to equation 1.

$$\text{Gain} = R_F/R_I \quad (1)$$

The internal feedback resistors (R_F) are trimmed to 40 kΩ.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

Bypass Capacitor (C_{BYPASS}) and Start-Up Time

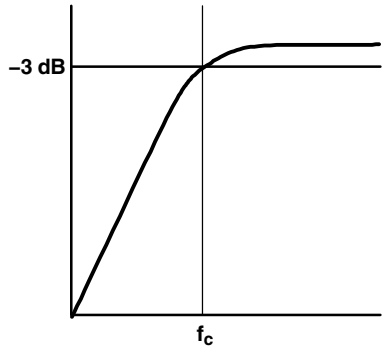
The internal voltage divider at the BYPASS pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to $V_{DD}/2$. Adding a capacitor to this pin filters any noise into this pin and increases k_{SVR}. $C_{(BYPASS)}$ also determines the rise time of V_{O+} and V_{O-} when the device is taken out of shutdown. The larger the capacitor, the slower the rise time. NO TAGNO TAGNO TAGNO TAGNO TAG show the relationship of $C_{(BYPASS)}$ to start-up time.

Input Capacitor (C_I)

The TPA6204A1 does not require input coupling capacitors if using a differential input source that is biased from 0.5 V to V_{DD} – 0.8 V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 2.

$$f_c = \frac{1}{2\pi R_I C_I} \quad (2)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 100 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (3)$$

In this example, C_I is 0.16 μF, so one would likely choose a value in the range of 0.22 μF to 0.47 μF. Ceramic capacitors should be used when possible, as they are the best choice in preventing leakage current. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (C_S)

The TPA6204A1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF to 1 μF, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a 10-μF or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

FULLY DIFFERENTIAL AMPLIFIER EFFICIENCY AND THERMAL INFORMATION

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the average value of the supply current, $I_{DD}(avg)$, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 18).

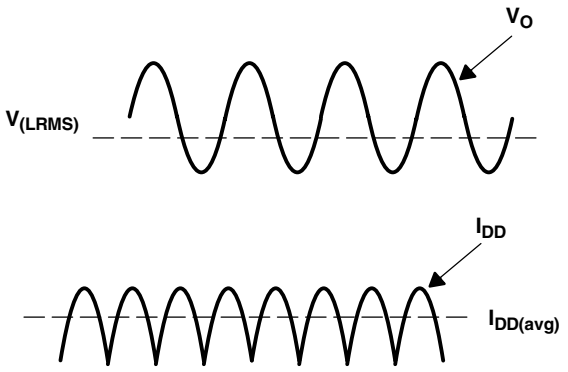


Figure 18. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \quad (4)$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = -\frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into equation 6,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L\, R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}} \quad (5)$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 2 and Table 3 employ equation (5) to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 1.6 W.

A final point to remember about Class-AB amplifiers is how to manipulate the terms in the efficiency equation to the utmost advantage when possible.

A simple formula for calculating the maximum power dissipated, P_{Dmax}, may be used for a differential output application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (6)$$

P_{Dmax} for a 5-V, 8-Ω system is 0.64 W.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the 3 mm x 3 mm DRB package is shown in the dissipation rating table. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0218} = 45.9°C/W \quad (7)$$

Given Θ_{JA}, the maximum allowable junction temperature, and the maximum internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA6204A1 is 150°C.

$$T_A\,Max = T_J\,Max - \Theta_{JA}\,P_{Dmax} \quad (8)$$
$$= 150 - 45.9(0.64) = 120.6°C$$

Equation (8) shows that the maximum ambient temperature is 120.6°C (package limited to 85°C) at maximum power dissipation with a 5-V supply.

Table 2 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA6204A1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. In addition, using speakers with an impedance higher than 8-Ω dramatically increases the thermal performance by reducing the output current.

Table 2. Efficiency and Maximum Ambient Temperature vs Output Power in 3.6-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Internal Dissipation (W)	Power From Supply (W)	Max Ambient Temperature (2) (°C)
0.1	27.6	0.262	0.36	85
0.2	39.0	0.312	0.51	85
0.5	61.7	0.310	0.81	85
0.6	67.6	0.288	0.89	85

(1) DRB package
(2) Package limited to 85°C ambient

Table 3. Efficiency and Maximum Ambient Temperature vs Output Power in 5-V 8-Ω Systems

Output Power (W)	Efficiency (%)	Internal Dissipation (W)	Power From Supply (W)	Max Ambient Temperature (2) (°C)
0.5	44.4	0.625	1.13	85
1	62.8	0.592	1.60	85
1.36	73.3	0.496	1.86	85
1.7	81.9	0.375	2.08	85

(1) DRB package
(2) Package limited to 85°C ambient

PCB LAYOUT

It is important to keep the TPA6204A1 external components very close to the TPA6204A1 to limit noise pickup.

8-Pin QFN (DRB) Layout

Use the following land pattern for board layout with the 8-pin QFN (DRB) package. Note that the solder paste should use a hatch pattern to fill solder paste at 50% to ensure that there is not too much solder paste under the package.

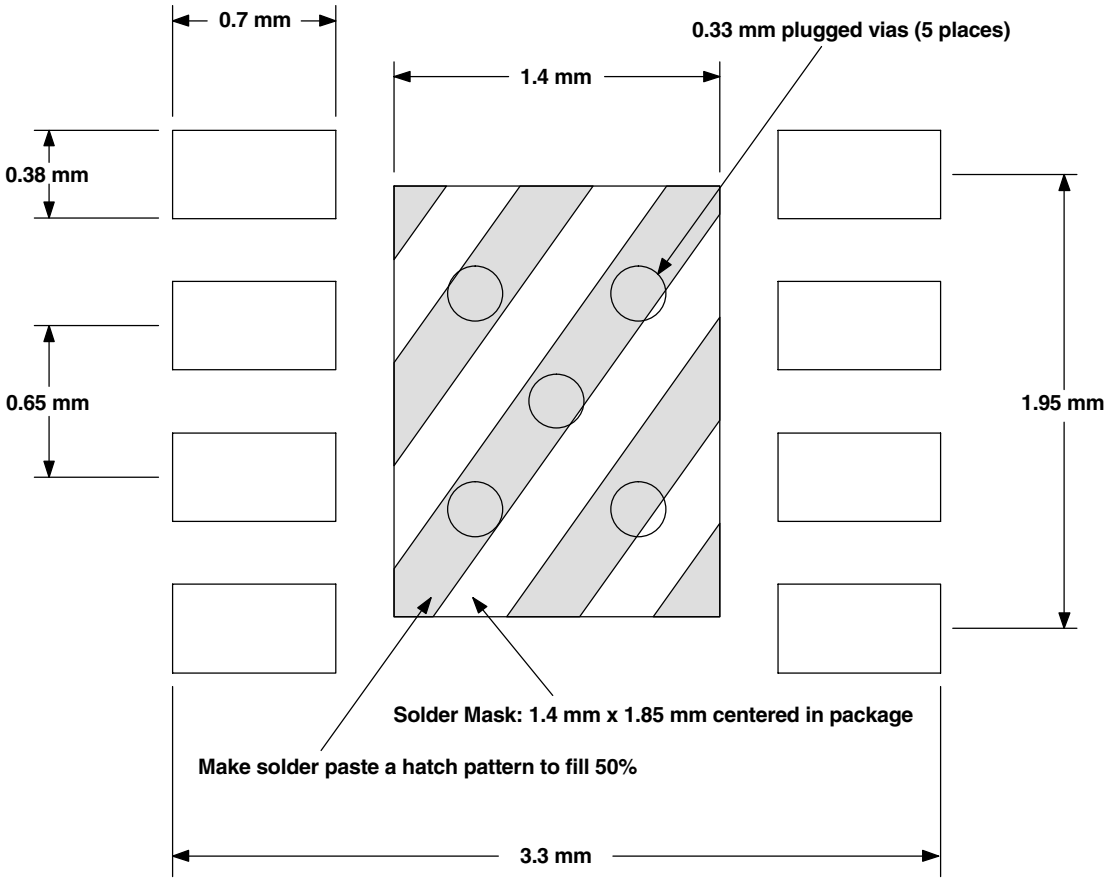


Figure 19. TPA6204A1 8-Pin QFN (DRB) Board Layout (Top View)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPA6204A1DRB	ACTIVE	SON	DRB	8	121	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA6204A1DRBG4	ACTIVE	SON	DRB	8	121	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA6204A1DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA6204A1DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

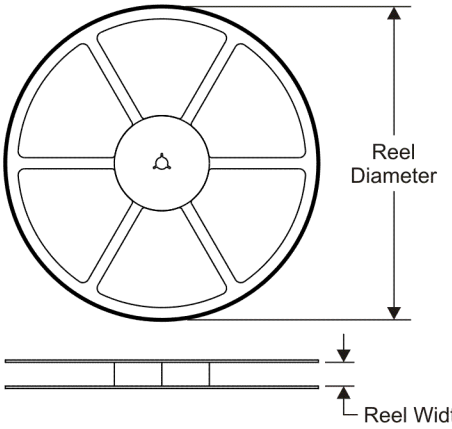
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

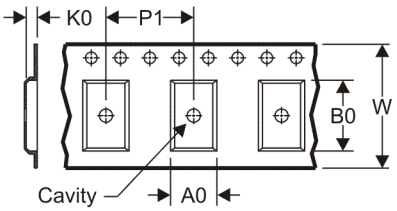
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

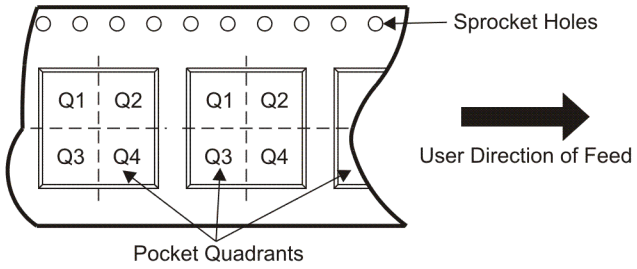


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

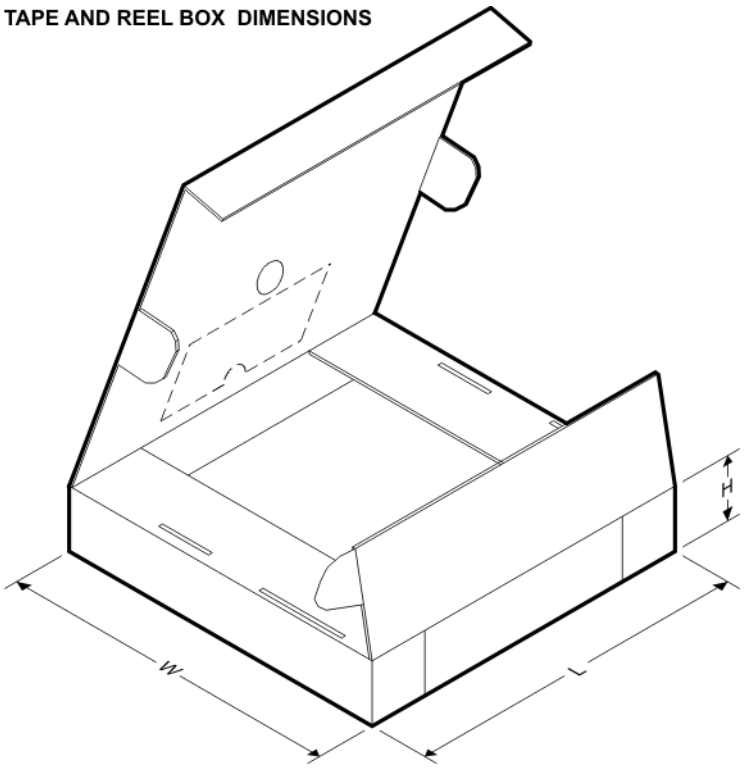
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6204A1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

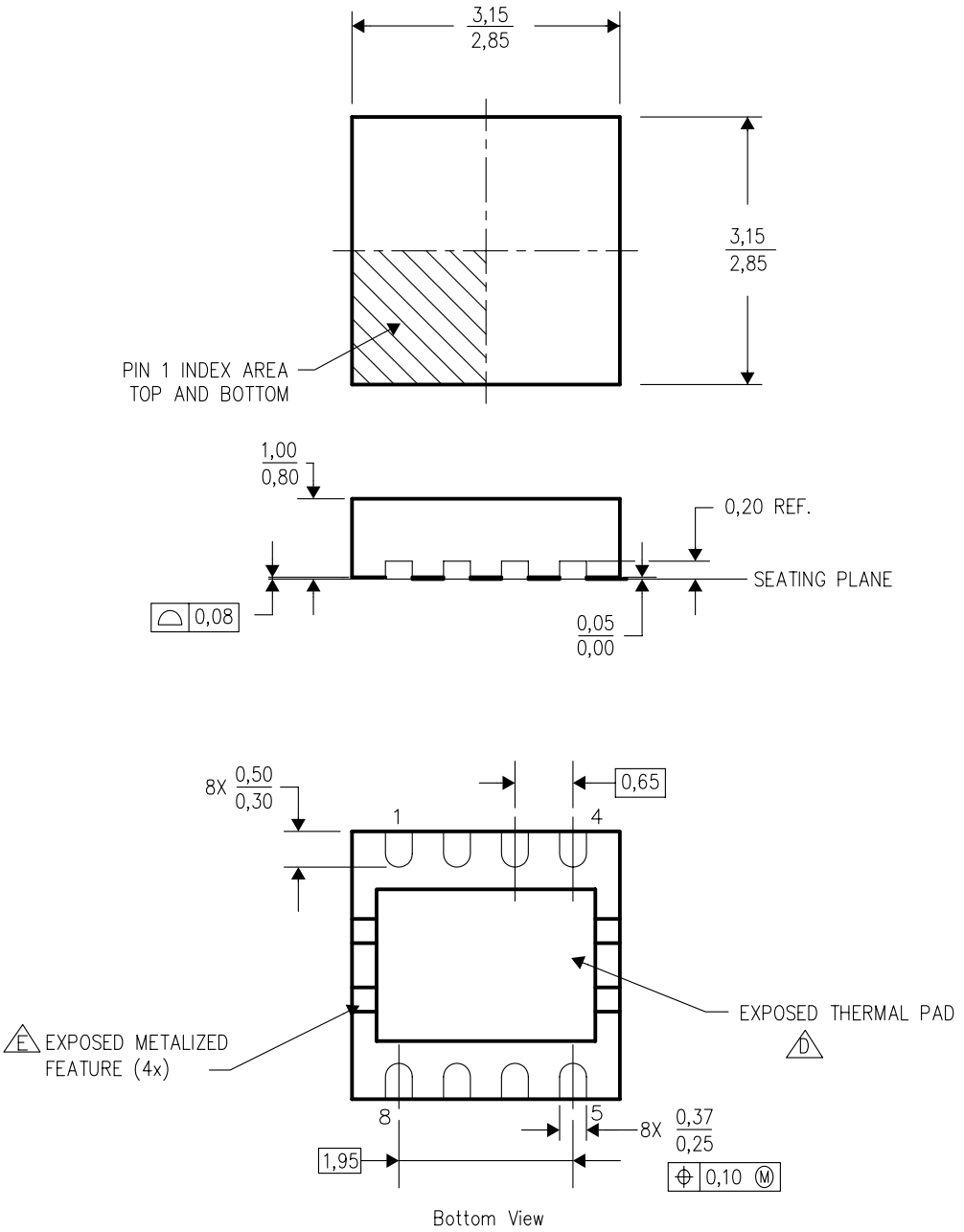
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6204A1DRBR	SON	DRB	8	3000	346.0	346.0	29.0

DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



4203482/G 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL PAD MECHANICAL DATA

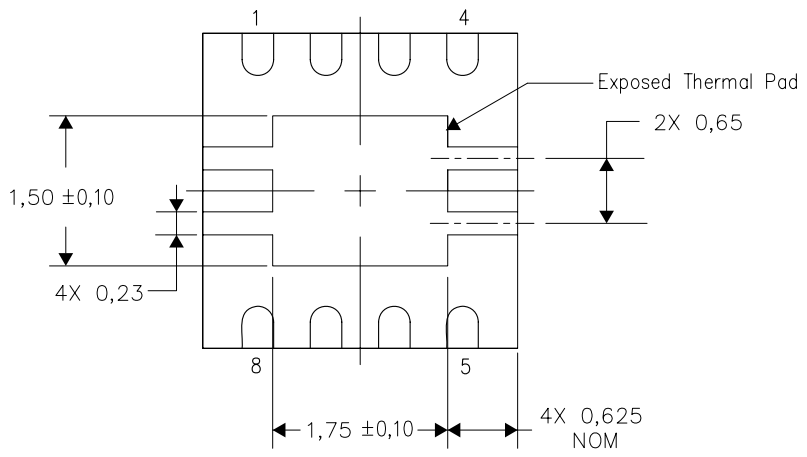
DRB (S–VSON–N8)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

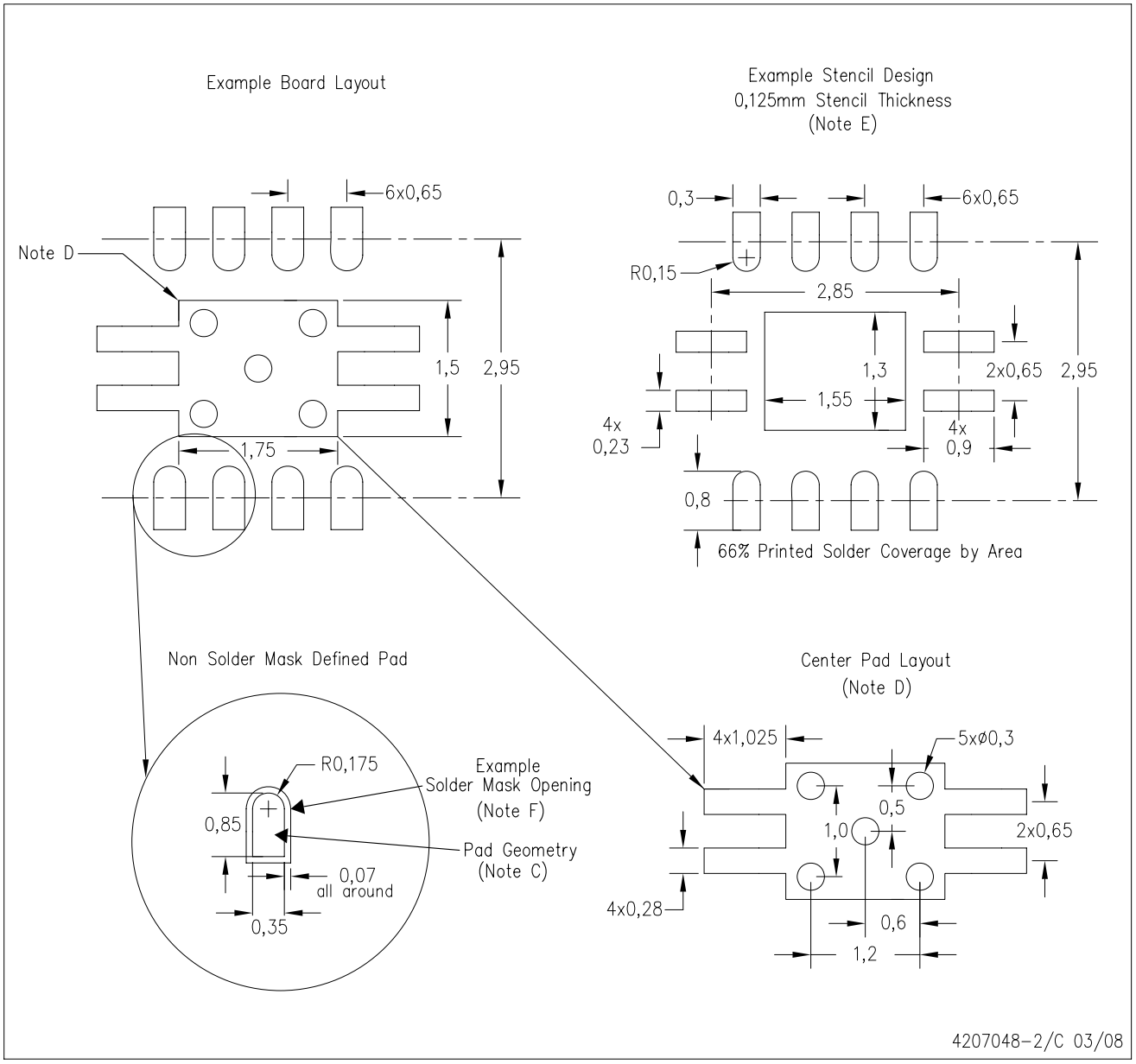


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRB (S–VSON–N8)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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